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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,829	09/25/2003	Jun Fan	11439 (NCR.0113US)	7323

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John D. Cowart
NCR Corporation
Law Department IP WHQ-4W
1700 S. Patterson Blvd.
Dayton, OH 45479

EXAMINER	
PATEL, ISHWARBHAI B	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 06/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/670,829	FAN ET AL.	
	Examiner	Art Unit	
	Ishwar (I. B.) Patel	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *11,12 and 20-26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 13-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: Appendix "A"

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 18, 2006 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-10 and 13-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asahi (US Patent No. 6,975,516) in view of Smith (US Patent No. 6,340,796).

Regarding claim 1, Asahi, in figure 8, discloses a circuit board comprising: first and second reference plane layers (first and second reference plane layers as marked on figure 8 in appendix "A") where the inner surface of each layer is separated by and in

contact with a dielectric layer (dielectric layer between the first and second reference plane layer, see Appendix "A");

an embedded discrete surface mount first decoupling capacitor (804-1,see appendix "A") mounted to the outer surface of the first reference plane layer (see appendix "A"), the first decoupling capacitor comprising a first electrode connected to the first reference plane (electrode of the capacitor 804-1a connected to the first reference plane layer, see appendix "A") and second electrode connected to the second reference plane layer (see appendix "A");

an embedded discrete surface mount second decoupling capacitor (804-2a, see appendix "A") mounted to the outer surface of the second reference plane layer, the second decoupling capacitor comprising a first electrode connected to the second reference plane (electrode of the second capacitor 804-2a connected to the second reference layer, see appendix "A") and a second electrode connected to the first reference plane (see appendix "A"); and

via extending generally along direction perpendicular to the first and second reference plane layers (via not labeled, one shown on the right side of figure 8, as only part section of the structure is shown),

wherein the first and second decoupling capacitor are aligned generally along the direction and overlapping one another (see appendix "A") to increase an amount of space in the circuit board through which the via are extendable.

Asahi does not explicitly discloses multiple vias extending generally along direction perpendicular to the first and second reference plane layers. Asahi, in figure 8,

only shows part cross-section of the board with one via on the right side of the figure. However, multiple vias are known in the art to facilitate various connection in and on the surface of the circuit board. Smith, in figure 2, discloses a structure with multiple via holes (48) extending between the layers providing electrical connection.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to construe the circuit board structure of Asahi with a multiple vias, from the teaching of Smith, in order to facilitate various electrical connections.

Regarding claim 2, the modified assembly of Asahi further discloses the vias comprise through-hole vias that extend from one side of the circuit to another side of the circuit board, (one shown on right side of partial figure 8 and Smith figure 2).

Regarding claim 3, the modified assembly of Asahi further discloses additional first decoupling capacitors (804-1b) mounted to the outer surface of the first reference plane layer (see appendix "A", capacitor on the right of the figure), and additional second decoupling capacitors (804-2b) mounted to the outer surface of the second reference plane layer (see appendix "A", capacitor on right of the figure), wherein each pair of first and second decoupling capacitors are aligned generally along the direction such that multiple spaced-apart lines of decoupling capacitors are provided, each line of decoupling capacitors including a respective pair of first and second decoupling capacitors (see appendix "A").

Regarding claim 4, the modified assembly of Asahi further discloses the vias extend through the circuit board in regions devoid of decoupling capacitors, (one shown on right in figure 8).

Regarding claim 5, the modified assembly of Asahi further discloses the first and second decoupling capacitors are separated by at least the first and second reference plane layers and the dielectric layer (see appendix "A"), and the vias extend through the first and second reference plane layers and the dielectric layer (see appendix figure 8).

Regarding claim 6, the modified assembly of Asahi further discloses each of the first decoupling capacitors includes a first electrode and a second electrode (see Appendix "A"), the circuit board further comprising a first buried via (for example, first buried via on left of first decoupling capacitor 804-1a) electrically contacted to the first electrode of one of the first decoupling capacitors (see appendix "A"), the first buried via extending through the first reference plane layer and the dielectric layer to electrically contact the second reference plane layer (see appendix "A").

Regarding claim 7, the modified assembly of Asahi further discloses each of the second decoupling capacitors (803-2a, 2b) includes first and second electrodes (see appendix "A"), the circuit board further comprising a second buried via (for example,

second buried via on right of second decoupling capacitor 804-2a, 2b) electrically contacted to the first electrode of one of the second decoupling capacitors (see appendix "A"), the second buried via extending through the second reference plane layer and dielectric layer to electrically contact the first reference plane layer (see appendix "A").

Regarding claim 8, the modified assembly of Asahi further discloses layers provided above and below a core assembly including the first and second reference plane layers, dielectric layer, and first and second decoupling capacitors (figure 8, Asahi).

Regarding claim 9, the modified assembly of Asahi further discloses the first decoupling capacitors are spaced apart with respect to each other across the outer surface of the first reference plane layer, and the second decoupling capacitors are spaced apart with respect to each other across the outer surface of the second reference plane layer (see Asahi figure 8 in appendix "A").

Regarding claim 10, the modified assembly of Asahi further discloses first regions between the spaced apart first decoupling capacitors (region between the capacitors 804-1a, 1b, see appendix "A"); and second regions between the spaced apart second decoupling capacitors (region between capacitors 804-2a, 2b, see appendix "A"), the first and second regions being generally aligned along the direction,

the vias extending through the circuit board through the first and second regions, (Figure 8 of Asahi in appendix "A").

Regarding claim 13, the modified assembly Asahi discloses all the features of the claimed invention including the first and second reference plane layers where the inner surface of each layer is separated by and attached to a dielectric layer; and embedded discrete surface mount first and second decoupling capacitors, as applied to claim 1 above and further recites integrated circuit device (806, 811, figure 8). Regarding the limitation "a power supply", though the modified system of Asahi does not explicitly disclose a power supply, the power supply has to be there for operating the system. Therefore, the modified assembly of Asahi meets the limitations.

Regarding claim 14, the modified assembly of Asahi further discloses the vias comprise through-hole vias that extend from one side of the circuit board to another side of the circuit board, as applied to claim 2 above.

Regarding claim 15, the modified assembly of Asahi discloses all the features of the claimed invention as applied to claim 13 above including the through vias extending through the circuit board in regions between spaced apart first and second decoupling capacitors as applied to claims 4 and 5 above.

Regarding claim 16, the modified assembly of Asahi discloses all the features of the claimed invention including the circuit board further comprising each of the first decoupling capacitors includes a first electrode and a second electrode and wherein the circuit board further comprises a first buried via electrically contacted to the first electrode of one of the decoupling capacitors, the first buried via extending through the first reference plane layer and the dielectric layer to electrically contact the second reference plane layer as applied to claim 6 above.

Regarding claim 17, the modified assembly of Asahi discloses all the feature of the claimed invention including each of the second decoupling capacitors includes first and second electrodes, wherein the circuit board further comprises a second buried via electrically contacted to the first electrode of one of the second decoupling capacitors, the second buried via extending through the second reference plane layer and dielectric layer to electrically contact the first reference plane layer as applied to claim 7 above.

Regarding claim 18, the modified assembly of Asahi further discloses all the features of the claimed invention the layers provided above and below a core assembly including the first and second reference plane layers, dielectric layer, and first and second decoupling capacitors, as applied to claim 8 above.

Regarding claim 19, the modified assembly Asahi further discloses first regions between the spaced apart first decoupling capacitors and second regions between the

spaced apart second decoupling capacitors, the first and second regions being generally aligned along the direction, the vias extending through the circuit board through the first and second region, as applied to claim 10 above.

4. Claims 1-3, 5, 8, 9, 13, 14 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blakely (US Patent No. 6,618,266) in view of Hayashi (US Patent No. 6,809,268).

Regarding claim 1, Blakely, in figure 3-6, discloses a circuit board comprising: first (102c) and second (102d) reference plane layers, where the inner surface of each layer is separated by and in contact with a dielectric layer (dielectric layer between 102c and 102d);

A discrete surface mount first decoupling capacitor (104a) mounted to the outer surface of the first reference plane layer (102c), the first decoupling capacitor comprising a first electrode connected to the first reference plane (102c) and second electrode connected to the second reference plane layer (102d);

a discrete surface mount second decoupling capacitor (104c) mounted to the outer surface of the second reference plane layer, the second decoupling capacitor comprising a first electrode connected to the second reference plane (102d) and a second electrode connected to the first reference plane (102c); and

via extending generally along direction perpendicular to the first and second reference plane layers (see figure 4 -6).

wherein the first and second decoupling capacitor are aligned generally along the direction and overlapping one another (see figure 3).

Blakely do not disclose the decoupling capacitors are embedded capacitors. Blakely discloses just the assembly of the capacitors. However, use of such assembly of capacitors into the circuit board assembly is known in the art to increase the available surface area of the board. Hayashi discloses a circuit board with capacitors (10) embedded into the circuit board.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to have the assembly of Blakely used in the circuit board causing the capacitor to be embedded capacitors, as taught by Hayashi, in order to increase the available surface area of the board.

Regarding claim 2, the modified assembly of Blakely further discloses the vias comprise through-hole vias that extend from one side of the circuit to another side of the circuit board, (see figure 4-6).

Regarding claim 3, the modified assembly of Blakely further discloses additional first decoupling capacitors (104b) mounted to the outer surface of the first reference plane layer (see figure 3), and additional second decoupling capacitors (104d) mounted to the outer surface of the second reference plane layer (see figure 3), wherein each pair of first and second decoupling capacitors are aligned generally along the direction such that multiple spaced-apart lines of decoupling capacitors are provided, each line of

decoupling capacitors including a respective pair of first and second decoupling capacitors (see figure 3)

Regarding claim 5, the modified assembly of Blakely further discloses the first and second decoupling capacitors are separated by at least the first and second reference plane layers and the dielectric layer (see figure 3) and the vias extend through the first and second reference plane layers and the dielectric layer (see figure 6).

Regarding claim 8, the modified assembly of Blakely further discloses layers provided above and below a core assembly including the first and second reference plane layers, dielectric layer, and first and second decoupling capacitors (see Hayashi figure 1A).

Regarding claim 9, the modified assembly of Blakely further discloses the first decoupling capacitors are spaced apart with respect to each other across the outer surface of the first reference plane layer, and the second decoupling capacitors are spaced apart with respect to each other across the outer surface of the second reference plane layer (see Blakely, figure 3)

Regarding claim 13, the modified assembly Blakely discloses all the features of the claimed invention including the first and second reference plane layers where the inner surface of each layer is separated by and attached to a dielectric layer; and

embedded discrete surface mount first and second decoupling capacitors, as applied to claim 1 above and further recites integrated circuit device (Hayashi, figure 1A, element 34). Regarding the limitation "a power supply", though the modified system of Blakely does not explicitly disclose a power supply, the power supply has to be there for operating the system. Therefore, the modified assembly of Asahi meets the limitations.

Regarding claim 14, the modified assembly of Blakely further discloses the vias comprise through-hole vias that extend from one side of the circuit board to another side of the circuit board, as applied to claim 2 above.

Regarding claim 18, the modified assembly of Blakely further discloses all the features of the claimed invention the layers provided above and below a core assembly including the first and second reference plane layers, dielectric layer, and first and second decoupling capacitors, as applied to claim 8 above.

Response to Arguments

5. Applicant's arguments with respect to claims 1-10 and 13-19 have been considered but are moot in view of the new ground(s) of rejection.

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

IP
June 23, 2006

IBPatel

ISHWAR PATEL
PRIMARY EXAMINER